

 <div data-bbox="491 98 539 264" style="display: inline-block; vertical-align: middle;"> <b>I Q R</b> </div>	IBIS QUALITY REPORT	date	1 (8)
		22-Nov-16	

## IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m93xxx_c6_tssop8.ibs
IBIS Version:	4.0

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# 1. MODELING

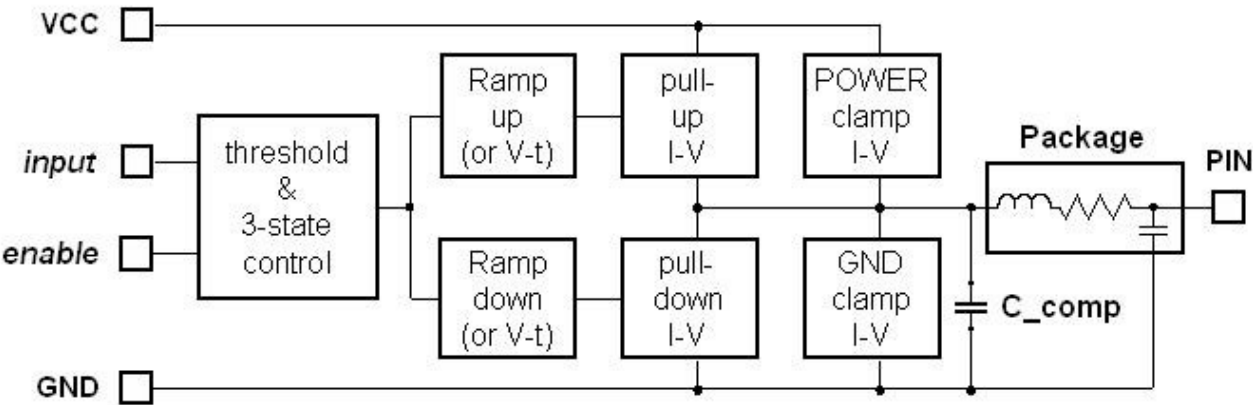
IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

## 1.1 Component description

Component name	Technology	Component description
M93Cx6–R or -W	CMOS F8H/P2	The M93xxx- is a serial SPI bus EEPROM Memory with high-speed clock. This IBIS model is the same for either the 16Kb (M93C86-R or -W), 8Kb (M93C76-R or -W), 4Kb (M93C66-R or -W), 2Kb (M93C56-R or -W) or 1Kb (M93C46-R or -W) in TSSOP8 package.

## 1.2 Modeling conditions

Simulator used	AMS 2010.1 (Mentor Graphics)
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**Figure 1:** IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	85
Voltage Supply [Volt]	5.00	4.50	5.50
Process setting	nom	weak	strong

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<b>Model names</b> (of Component)	<b>Model Type</b>	<b>C_comp (typ, min, max)</b>
mod_s	Input	2.119pF (typ), 2.024pF(min) , 2.324pF(max)
mod_q	I/O	2.668pF (typ), 2.548pF (min) , 2.925pF(max)
mod_w	Input	2.119pF (typ), 2.024pF(min) , 2.324pF(max)
mod_h	Input	2.119pF (typ), 2.024pF(min) , 2.324pF(max)

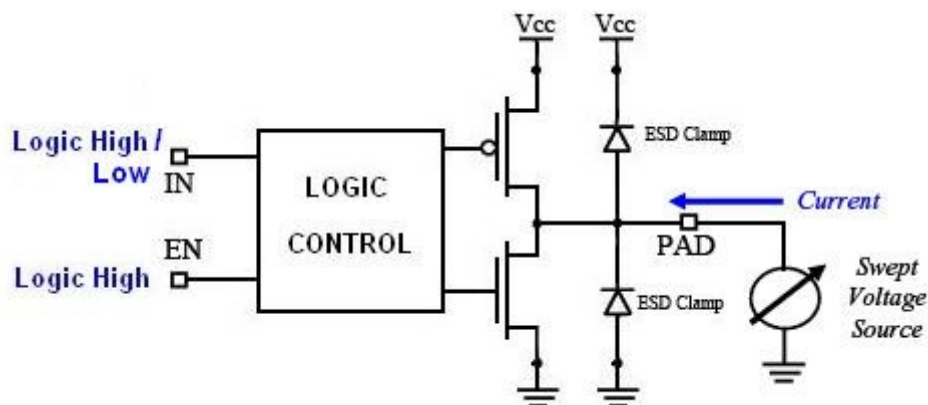
<b>Model names</b> (of Component)	<b>Threshold and Vmeas</b>	<b>Timing parameters (if used)</b>
mod_scl/wc/en	Vil=1.250V , Vih=3.750V	
mod_sda	Vmeas=2.500V	Cref=30pF

<b>Package</b>	<b>Description</b>
TSSOP8	8 pin thin shrink small outline

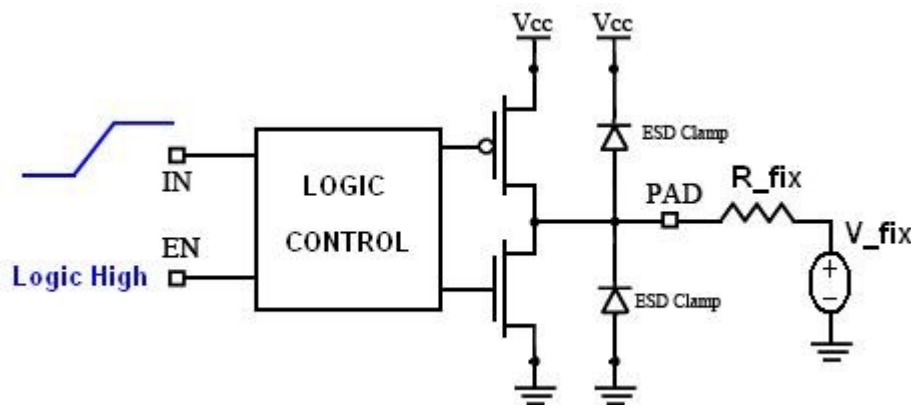
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### 1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.



**Figure 2:** Simulation Setup to extract *I/V* data from I/O model type



**Figure 3:** Simulation Setup to extract *V/T* data from I/O model type (see also Table 1)

<b>V/T data condition extractions</b>	<b>Load conditions</b>
Rising waveform	$R_{fix}=50\text{ Ohm}$ , $V_{fix}= 0\text{ V}$
Rising waveform	$R_{fix}=50\text{ Ohm}$ , $V_{fix}= 5.0\text{ V}$
Falling waveform	$R_{fix}=50\text{ Ohm}$ , $V_{fix}= 5.0\text{ V}$
Falling waveform	$R_{fix}=50\text{ Ohm}$ , $V_{fix}= 0\text{ V}$

**Table 1:** V/T curve extraction load conditions

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## 2. IBISCHK6 CHECK

The created IBIS model must be checked using IBISCHK6 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

### 2.1 Result Check by IBISCHK6

*IBISCHK6 V6.0.1*

*Checking m93xxx\_c6\_tssop.ibs for IBIS 4.2 Compatibility...*

*NOTE (line 298) - Pulldown Typical data is non-monotonic*

*NOTE (line 298) - Pulldown Minimum data is non-monotonic*

*NOTE (line 299) - Pulldown Maximum data is non-monotonic*

*NOTE (line 395) - Pullup Typical data is non-monotonic*

*NOTE (line 395) - Pullup Maximum data is non-monotonic*

*NOTE (line 396) - Pullup Minimum data is non-monotonic*

*Errors : 0*

*File Passed*

#### **Adding comments about the Warning or Note:**

The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.

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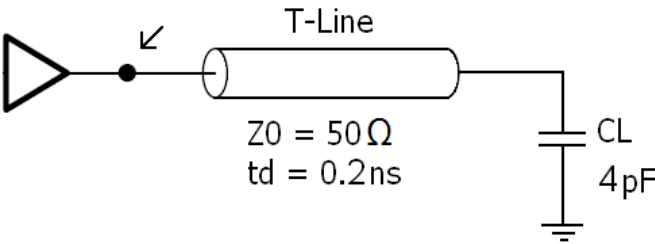
### 3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions ( Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put “X” into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions.	
Curves match well.	<b>X</b>

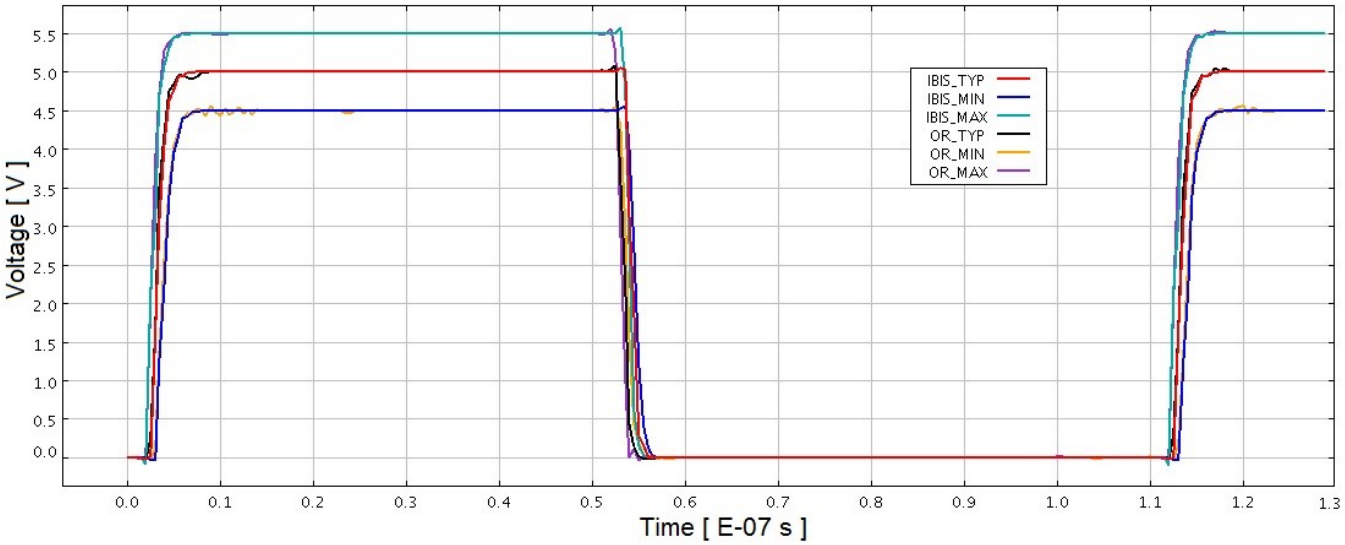
#### 3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.



**Figure 4:** Circuit used for functional check

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**Figure 5:** IBIS vs Eldo comparison results of “mod\_q” Model

Output Comparisons:

<b>Adding comments about the comparison:</b>

#### 4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

Other specifications	description